WHAT IS CLAIMED IS:

1. A method of quantifying the stability of a placement tool used in mapping the physical layout of logic cells for an integrated circuit chip, comprising the steps of:

designing a first layout of logic cells using the placement tool based on a first set of input parameters;

designing a second layout of the logic cells using the placement tool based on a second set of input parameters which is different from the first set of input parameters; and

calculating a stability value based on the movement of respective cell locations from the first layout to the second layout.

2. The method of Claim 1 wherein said calculating step includes the step of normalizing the stability value based on respective cell locations in a third layout which is a random placement of the logic cells.

3. The method of Claim 1 wherein said calculating step measures absolute movement of individual logic cells.

4. The method of Claim 3 wherein cell movement is weighted by cell area in calculating the stability value.

5. The method of Claim 3 wherein absolute cell movement is squared in calculating the stability value.

6. The method of Claim 1 wherein said calculating step measures relative movement of logic cells with respect to the one or more nets of the layouts.

7. The method of Claim 6 wherein shifting of logic cells and symmetric reversal of logic cells about a net center does not contribute to the relative movement, but

spreading of logic cells and rotation of logic cells with respect to the net center does contribute to the relative movement.

8. The method of Claim 6 wherein relative cell movement is squared in calculating the stability value.

9. The method of Claim 1 wherein the placement tool uses an annealing algorithm, and the first and second sets of input parameters have different annealing schedules.

10. The method of Claim 1 wherein the placement tool uses a multi-level algorithm, and the first and second sets of input parameters have different random seeds for clustering.

11. The method of Claim 1 wherein the placement tool uses a quadratic algorithm, and the first and second sets of input parameters have different stopping criteria.

12. A computer system comprising:

means for processing program instructions;

a memory device connected to said processing means; and

program instructions residing in said memory device for quantifying the stability of a placement tool used in mapping the physical layout of logic cells for an integrated circuit chip, wherein said program instructions design a first layout of logic cells using the placement tool based on a first set of input parameters, design a second layout of the logic cells using the placement tool based on a second set of input parameters which is different from the first set of input parameters, and calculate a stability value based on the movement of respective cell locations from the first layout to the second layout.

13. The computer system of Claim 12 wherein said program instructions normalize the stability value based on respective cell locations in a third layout which is a random placement of the logic cells.

14. The computer system of Claim 12 wherein said program instructions measure absolute movement of individual logic cells.

15. The computer system of Claim 14 wherein said program instructions weight cell movement by cell area in calculating the stability value.

16. The computer system of Claim 14 wherein said program instructions square absolute cell movement in calculating the stability value.

17. The computer system of Claim 12 wherein said program instructions measure relative movement of logic cells with respect to the one or more nets of the layouts.

18. The computer system of Claim 17 wherein shifting of logic cells and symmetric reversal of logic cells about a net center does not contribute to the relative movement, but spreading of logic cells and rotation of logic cells with respect to the net center does contribute to the relative movement.

19. The computer system of Claim 17 wherein said program instructions square relative cell movement in calculating the stability value.

20. A computer program product comprising:

a computer-readable medium; and

program instructions residing in said medium for quantifying the stability of a placement tool used in mapping the physical layout of logic cells for an integrated circuit chip, wherein said program instructions design a first layout of logic cells using the placement tool based on a first set of input parameters, design a second layout of the logic cells using the placement tool based on a second set of input parameters which is different from the first set of input parameters, and calculate a stability value based on the movement of respective cell locations from the first layout to the second layout.

21. The computer program product of Claim 20 wherein said program instructions normalize the stability value based on respective cell locations in a third layout which is a random placement of the logic cells.

22. The computer program product of Claim 20 wherein said program instructions measure absolute movement of individual logic cells.

23. The computer program product of Claim 23 wherein said program instructions weight cell movement by cell area in calculating the stability value.

24. The computer program product of Claim 23 wherein said program instructions square absolute cell movement in calculating the stability value.

25. The computer program product of Claim 20 wherein said program instructions measure relative movement of logic cells with respect to the one or more nets of the layouts.

26. The computer program product of Claim 25 wherein shifting of logic cells and symmetric reversal of logic cells about a net center does not contribute to the relative movement, but spreading of logic cells and rotation of logic cells with respect to the net center does contribute to the relative movement.

27. The computer program product of Claim 25 wherein said program instructions square relative cell movement in calculating the stability value.